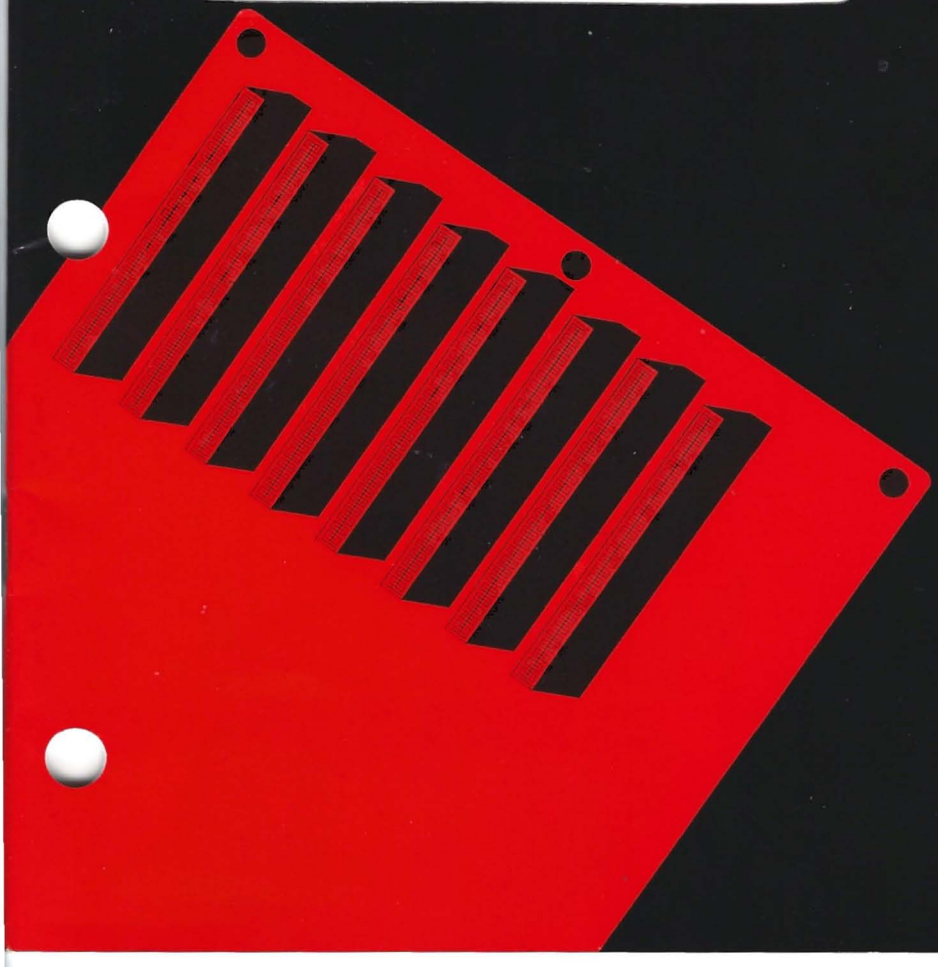
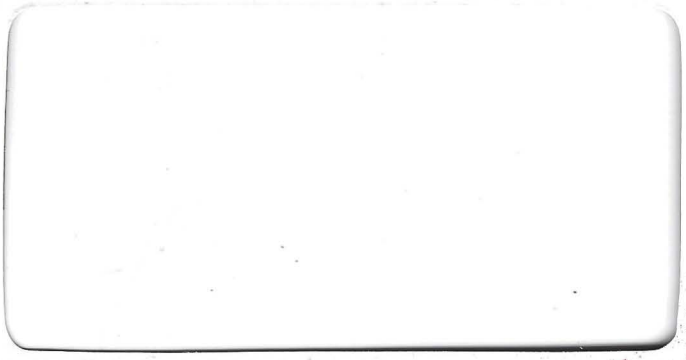
8088 MAIN BOARD

TXM/10-II M8031

TXM/8-III M8021





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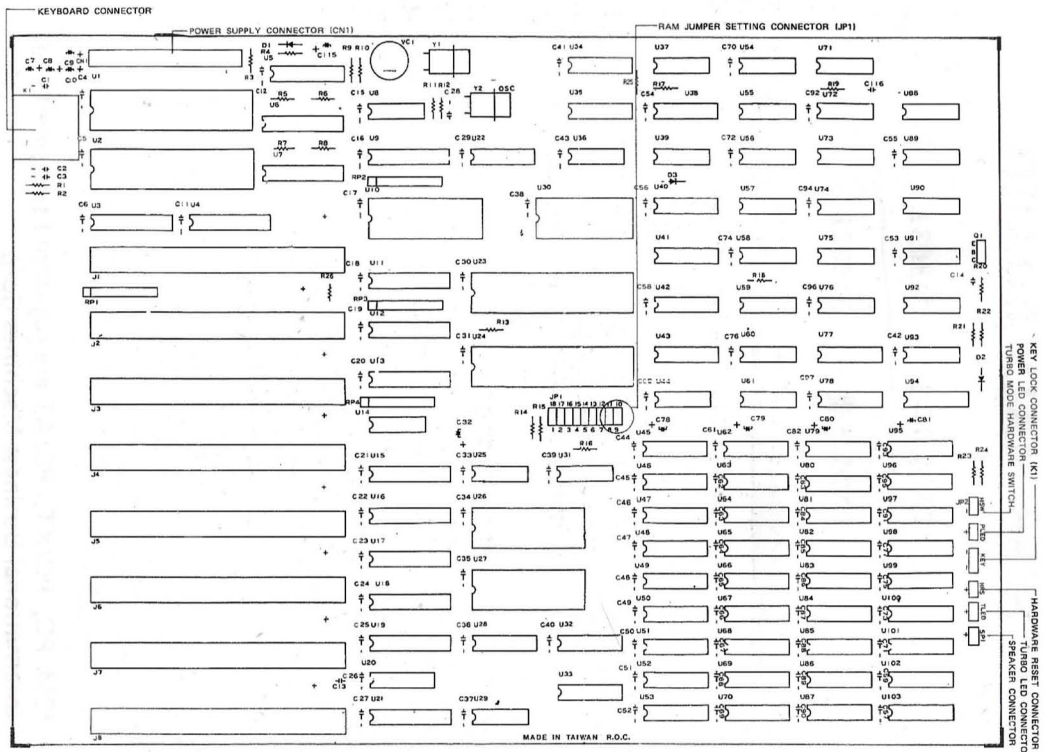

KEYBOARD CONNECTOR
POWER SUPPLY CONNECTOR (CN1)
RAM JUMPER SETTING CONNECTOR (JP1)
KEY LOCK CONNECTOR (K1)
POWER LED CONNECTOR
TURBO MODE HARDWARE SWITCH
HARDWARE RSSET CONNECTOR
TURBO LED CONNECTOR
SPEAKER CONNECTOR
MADE IN TAIWAN R.O.C.

TABLE OF CONTENTS

CHAPTER 1
THE NORMAL/TURBO MODE OPERATION

1.1 ADVANTAGES OF THE TURBO MAIN BOARD

The difference between the Turbo main board and other 8088 main boards is that the Turbo main board allows an increase of about 110% in speed of program execution. As the 8088-1 (8088-2) or qualified V20 processor operates at a quicker speed at 10MHz (8MHz). In other 8088 main board, the clock speed is only 4.77MHz.

The Turbo main board consists of a dual clock system. In Normal mode, the clock speed is only 4.77 MHz cycle. In Turbo mode, the clock speed increases to 10 MHz (8 MHz) cycle.

Note No. 1: Please do not make use of RAM memory on interface card. Because its original design may not be compatible with 10 MHz high speed CPU at access time. *Please use memory on mainboard and use 4164 or 41256 with access time within 120 ns.

For Example:

	4164–12	41256–12
NEC	D4164C–12	D41256–12
MITSUBISHI	M5K4164–12	M5M4256P–12
SIEMENS	HYB4164–12	HYB41256–12

1-2 To Obtain Turbo Mode

The system board supports both software switch as well as hardware switch to allow transaction between Normal mode (4.77MHz) and Turbo mode (10MHz or 8MHz).

A) Software Switch:

Let the hardware switch (HSW) be the status of "OPEN".

1) Turn on Turbo Mode:

Press and hold down the "CTRL" (CONTROL) and "ALT" (ALTERNATIVE) Keys and then press the "+" (plus) key then the cursor on screen display will appear as a "■" (box). Now, you are ready to use Turbo mode and the Turbo LED is on.

2) Press and hold down "CTRL" (CONTROL) and "ALT" (ALTERNATE) keys and then press the "+" (plus) key to come back to Normal mode at 4.77 MHz. You will see on screen display that the cursor shows up as a "—" (DASH) and the Turbo LED is off.

B) Hardware Switch:

Put a jumper on the HSW will turn on the turbo mode; otherwise, remove the jumper to set the system to be in normal mode.

1) Push button setting

If there is a push button switch on the front panel.

a) Turn on Turbo Mode

Push the Turbo switch into "ON" position to turn on Turbo mode at 10 MHz (or 8 MHz) If the Turbo LED is on it indicate system is in Turbo Mode now.

b) Return to Normal Mode:

Push the Turbo switch into "OFF" position to come back to Normal mode at 4.77 MHz and the Turbo LED is off.

If you want to use software switch to select speed you must first disconnect jumper HSW.

The Comparison Table of Turbo 8 MHz Main Board & Turbo 10 MHz Main Board.

Item	TXM/8	TXM/10
Microprocessor	8088-2	8088-1
Co-processor	8087-2	8087-1
System Clock	4.77/8 MHz	4.77/10 MHz
Memory Access Time	150 ns	120 ns
OSC	24 MHz	30 MHz

CHAPTER 2
CONNECTORS AND SWITCH SETTING

2-1 Connectors

A) Power Supply Connectors (CN1)

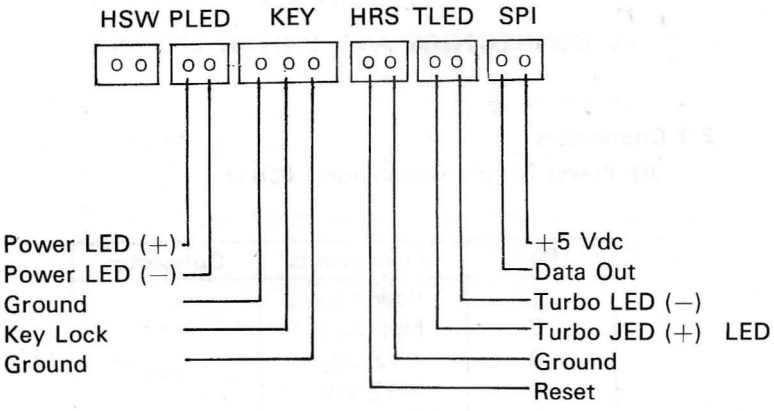
Pin	Assignments	Connector
1	Power good	CN1
2	Not used	
3	+ 12 Vdc	
4	– 12 Vdc	
5	Ground	
6	Ground	
7	Ground	CN1
8	Ground	
9	– 5 Vdc	
10	+ 5 Vdc	
11	+ 5 Vdc	
12	+ 5 Vdc	

B) Keyboard Connector (K1)

The keyboard connector is 5-pin, 90-degree, Printed Curcuit Board (PCB) mounting, DIN connector. The pin assignments are as follows:

Pin	Assignments
1	Keyboard clock
2	Keyboard data
3	Keyboard reset
4	Ground
5	+ 5 Vdc

(C) Jumper Connector (JP2):



NOTE: HSW—Please review chapter 1.

HRS—When this connector is open, the system is in regular operation.
When this connector is shorted for a while, the system restarts.

KEY—When "Keylock" is shorted with ground the keyboard is locked and can't key-in any command.

(d) Jumper Connector (JP1):

On Board Memory Setting.

11 10 [o o] [o o] 8 9	TOTAL 256K RAM
11 10 o [o o] o o 8 9	TOTAL 448K RAM
11 10 [o o] o o o o 8 9	TOTAL 640K RAM
11 10 o o o o o o 8 9	TOTAL 1024K RAM

2-2 THE SYSTEM BOARD SWITCH SETTING

The DIP Switch (SW1) is used to set the system configuration and specify the amount of memory installed on the system board. Generally the memory switch is useless now.

Position	Function
1	Normal operation off
2	User for 8087 co-processor
3-4	Amount of memory on system board
5-6	Type of display adapter
7-8	Number of 5¼ inch diskette drives

A) Switch 1 (U14)

1 = OFF (NORMAL OPERATION)
2 = ON W/O 8087-2 (8087-1) co-processor
2 = OFF W/ 8087-2 (8087-1) co-processor

Memory Switch Settings:

3 = OFF	4 = ON	128K MEMORY INSTALLED
3 = ON	4 = OFF	192K MEMORY INSTALLED
3 = OFF	4 = OFF	256K MEMORY INSTALLED

Display Adapter Switch Settings:

5 = ON	6 = ON	EGA DISPLAY ADAPTER
5 = OFF	6 = ON	COLOR/GRAPHICS (40x25 Mode)
5 = ON	6 = OFF	COLOR/GRAPHICS (80x25 Mode)
5 = OFF	6 = OFF	MONOCHROME DISPLAY ADAPTER OR BOTH

Display Dirve Switch Setting:

7 = ON	8 = ON	1 DRIVE INSTALLED
7 = OFF	8 = ON	2 DRIVES INSTALLED
7 = ON	8 = OFF	3 DRIVES INSTALLED
7 = OFF	8 = OFF	4 DRIVES INSTALLED

CHAPTER 3
MEMORY RAM/ROM CHIPS INSTALLATION

3-1 RAM Chip Installation

The 10 MHz (8MHz) mainboard provides 4 banks of memory.

BANK 0 U45 through U53

BANK 1 U62 through U70

BANK 2 U79 through U87

BANK 3 U95 through U103

* U45, U62, U79 and U95 are used for parity checking.

Option	RAM chips on Bank 0	RAM chips on Bank 1	RAM chips on Bank 2	RAM chips on Bank 3
256K RAM	4164x9	4164x9	4164x9	4164x9
448K RAM	41256x9	4164x9	4164x9	4164x9
640K RAM	41256x9	41256x9	4164x9	4164x9
1024K RAM	41256x9	41256x9	41256x9	41256x9

3-2 ROM CHIPS INSTALLATION

The 10 MHz (8MHz) Mainboard provides 2 ROM chips space for system.

S 27C64A-20 FA

U26 must be installed 2764 (27128) for ROM BIOS. Phoenix 735264

U27 must be installed 27256 for ROM BASIC.

Not applicable

3-3 RDISK.SYS (RAM-DISK) DEVICE DRIVER

The 10MHz main board allows you to use the expanded memory after 640K as a quick RAM-DISK.

The space of the virtual disk depends on the banks of 41256 RAM been set:

1) 3 banks of 41256 RAM → you have RAM-DISK spaces 128K.
2) 4 banks of 41256 RAM → you have RAM-DISK spaces 384K.

Getting started to create a CONFIG.SYS file to install the RDISK. SYS driver:

1) If you haven't a CONFIG.SYS file on your diskette, then create it; frist type in

COPY CON:CONFIG.SYS

Press ENTER key, Then type in

DEVICE=RDISK.SYS [Ctrl+Z] (or key in the function key F6)

Press ENTER key

The A> prompt displayed again and you have created a CONFIG.SYS file.

The screen display as follows:

```
A>COPY CON:CONFIG.SYS
     DEVICE=RDISK.SYS^Z
                    1 File(s) Copied
A>
```

2) If the CONFIG.SYS file already existed on your diskette, you will need to add one line to the file. You must have the line editor EDLIN program on your diskette.

Type in

EDLIN CONFIG.SYS

Press ENTER key, then type in

i

Press ENTER key, then type in

DEVICE=RDISK.SYS

Press ENTER key, then type in

[Ctrl+C]

Type in

e

Press ENTER key

The A> prompt displayed again. You have created a CONFIG.SYS file with driver RDISK.SYS in it.

The screen display as follows:

```
A>EDLIN CONFIG.SYS
*i
  1:*DEVICE=RDISK.SYS
  2:*^C
*e
A>
```

Once you have created the CONFIG.SYS file, DOS will install the RDISK.SYS driver in the CONFIG.SYS file to create RAM-DISK device. When you reset your system of course, you must have RDISK.SYS in your booting diskette.

The screen will display:

```
RDISK Ver 1.0 Copyright YANGTECH Electric Co., Ltd.
VIRTUAL DISK #: ### KB
```

With the RAM-DISK, you will get an excellent performance for programs need to access the disk frequently.

For example, if you save the compiler and source program to the virtual disk, the compiler time will be counted by seconds not by minutes; furthermore, the efficiency will be ten times higher without occupying the space of memory in 640K which is available for the user.

NOTE: You have to make sure that the data has been saved to a real disk before you turn your system power off because data will be erased.

CHAPTER 4 THE SYSTEM BOARD

4-1 Introduction

The 10MHz (8MHz) main board fits horizontally in the base of the system unit and is approximately 8½ x 12 inches. It is a double sided P.C.B. DC power and a signal from the power supply enters the board through two six-pin connectors. Other connectors on the board are for attaching the keyboard and speaker. Eight 62-pin card edge sockets are also mounted on the board. The I/O channel is bussed across these eight I/O slots.

A "Dual-in-Line Package (DIP) switch (SW1) (one eight switch pack) is mounted on the board and can be read under program control. The DIP switch provides the system software with information about the installed options, how much storage the system board has, what type of display adapter is installed, what operation modes are desired when power is switched on (color or black-and-white, 80- or 40-character lines), and the number of diskette drives attached.

The main board has five functions: the processor subsystem and its support elements, the Read Only Memory (ROM) subsystem the Read/Write (R/W) Memory subsystem, integrated I/O adapters, and the I/O channel.

The heart of the 10MHz (8MHz) main board is the INTEL 8088-1 (8088-2) or V20 microprocessor. This processor is an 8-bit external bus version of INTEL'S 16 bit 8086 processor, and is software compatible with the 8086. Thus, the 8088 supports 16 bit operations, including*, * multiplication and division and supports 20 bits addressing (1 megabyte of storage).

It also operates in amaximum mode, so a co-processor. can be added as a feature. The processor operates in two modes which can be switched, namely the Normal mode and the Turbo mode. When the processor is operating at 4.77MHz in the Normal mode, the frequency, which is derived from a 14.318MHz crystal, is divided by 3 for the processor clock, and by 4 to obtain the 3.58 MHz. color burts signal required for color teleyision. When the processor is operating in the 10 MHz (8MHz) Turbo mode, the frequency comes from a 30 MHz (24MHz) oscillator.

– DMA –

Three of the four DMA channels are available on the I/O bus and support high speed data transfers between I/O devices and memory without processor intervention. The fourth DMA channel is programmed to refresh the system dynamic memory. This is done by programming a channel of the timer counter device to request periodically a dummy DMA transfer. This action creates a memory-read cycle, which is available to refresh dynamic storage, both on the system board and in the system expansion slots. All DMA data transfers, except the refresh channel, take five proces sor clocks of 210 ns, or 1.05, μs it the processor ready line is not deactivated. Refreshing DMA cycles takes four clocks or 840 ns.

– INTERRUPT –

Of the eight prioritized levels of interrupt, six are bussed to the system expansion slots for use by feature cards. Two levels are used on the system board. Level 0, the highest priority, is attached to Channel 0 of the timer/counter and provides a periodic interrupt for the time-of-day clock. Level 1 is attached to the keyboard adapter circuits and receives an interrupt for each scan code sent by the keyboard. The Non-Maskable Interrupt (NMI) of the 8088 is used to report memory parity errors.

– MEMORY –

The main board supports both ROM/EPROM and R/W memory. It has space for 32K x 8 and 8K (16K) x 8 of ROM or EPROM. This ROM contains a power-on self-test, I/O drivers, dot patterns for 128 characters in graphics mode, and a diskette.

The main board also has from 64k to 1M bytes of R/W memory. A minimum system would have 64K of memory.

– KEYBOARD –

The main board contains the adapter circuits for attaching the serial interface from the keyboard. These circuits generate an interrupt to the processor, when a complete scan code is received. The interface can request execution of a diagnostic test in the keyboard.

The keyboard interface is a 5-pin DIN connector on the system board that extends through the rear panel of the system unit.

– SPEAKER –

The main unit has a 2¼-inch audio speaker. The speaker's control circuits and driver are on the system board. The speaker connects through a 2-wire interface that attaches to a 2-pin connector on the system board.

The speaker drive circuit is capable of providing approximately ½ watt of power. The control circuits allow the speaker to be driven three different ways: 1) a direct program control register bit may be toggled to generate a pulse train; 2) the output from Channel 2 of the timer counter may be programmed to generate a waveform to the speaker; 3) the clock input to the timer counter can be modulated with a program controlled by the I/O register bit. All three methods may be performed simultaneously.

4-2 Expansion I/O Channel

The I/O channel is an extension of the 8088 microprocessor bus. It is, however, demultiplexed, repowered, and enhanced by the addition of interrupts and Direct Memory Access (DMA) functions.

The I/O channel contains an 8 bit, bidirectional data bus, with 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines, a channel check line, and power and a ground for the adapters. Four voltage levels are provided for I/O cards. +5Vdc, −5Vdc, +12Vdc, and −12dc. These functions are provided in a 62-pin connector with 100-mil card-tab spacing.

A "ready" line is available on the I/O channel to allow operation with slow I/O or memory devices. If the channel's ready line is not activated by an addressed device, all processor-generated memory read and write cycles take four clocks. All processor-generated I/O read and write cycles requires five clocks. Refresh cycles occur once every 72 clocks and require four clocks or approximately 7% of the bus bandwidth.

I/O devices are addressed using I/O mapped address space. The channel is designed so that 768 I/O devices addressed are available to the I/O channel cards.

A channel check line exists for reporting error conditions to the processor. Activating this line results in a Non-Maskable Interrupt (NMI) to the 8088 processor. Memory expansion options use this line to report parity errors.

The I/O channel is repowered to provide sufficient drive, to power all eight (J8 to J4 and J3 to J1) expansion slots, assuming two Low-Power Schorttky (LS) loads per slot. The I/O adapters typically use only one load.

4-3 I/O Channel Description

The following is a description of the 10MHz (8MHz) system board I/O Channel. All lines are TTL-compatible.

I/O Signal Description

OSC, Oscillator:

High speed clock with a 70-ns period (14.31818 MHz). It has a 50% duty cycle.

CLK, System Clock:

It operates at one-third the frequency of the oscillator and has a period of 210 ns (4.77MHz) or 100 ns (10MHz); 150ns (8MHz). The clock has a 33% duty cycle.

RESET:

This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of the clock and is active high.

AO-A19, Address Bits 0 to 19:

These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 meg abyte of memory. AO is the Least Significant Bit (LSB) and A19 is the Most Significant Bit (MSB). These lines are generated by either the processor or the DMA controller. They are active high.

DO-D7, I/O Data Bits 0 to 7:

These lines provide data bus bits 0 to 7 for the processor,

memory, and I/O devices. DO is the Least Significant Bit (LSB) and D7 is the Most Significant Bit (MSB). These lines are active high.

ALE, Address Latch Enable:

This line is provided by the 8288 Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the falling edge of ALE.

$\overline{\text{I/O CH CK}}$, I/O Channel Check:

This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is indicated.

$\overline{\text{I/O CH RDY}}$, I/O Channel Ready:

This line, normally high (ready), can be pulled low (not ready) by a memory or an I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This line should never be held low longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles.

IRQ2-IRQ7, Interrupt Request 2 to 7:

These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is gener-

ated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor (interrupt service routine).

$\overline{\text{IOR}}$, I/O Read Command:

This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

$\overline{\text{IOW}}$, I/O Write Command:

This command line instructs an I/O device, to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

$\overline{\text{MEMR}}$, Memory Read Command:

This command line instructs the memory to drive its data into the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

$\overline{\text{MEMW}}$, Memory Write Command:

This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

DRQ1-DRQ3, DMA Request 1 to 3:

These lines are for asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding $\overline{\text{DACK}}$

line goes active.

$\overline{\text{DACK}}$ 0–3–DAM Acknowledge 0 to 3:

These lines are DACK3 used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK 0). They are active low.

AEN, Address Enable:

This line is used to degate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control over the address bus, the data bus, the read command lines (memory and I/O), and the write command lines (memory and I/O).

T/C, Terminal Count:

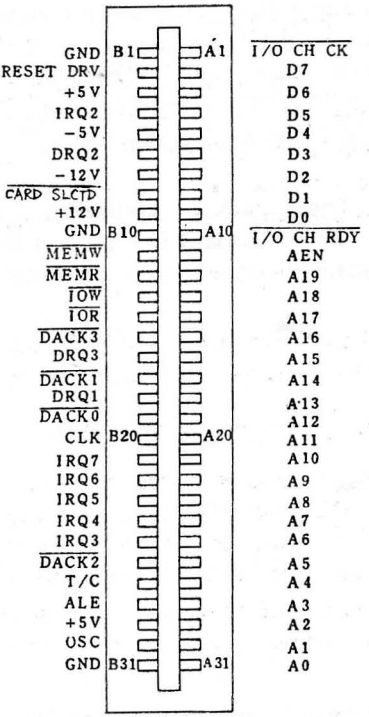
This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.

CARD SLCTD, Card Selected:

This line is activated by cards in expansion slot. It signals, "THE SYSTEM BOARD", that the card has been selected and that appropriate drivers on the system board should be directed to either read from, or write to, expansion slot. Connectors J8 to J4 and J3 to J1 are tied together at this pin, but the system board should be driven by an open collector device.

The following voltages are available on the system board I/O channel:

+5 Vdc +/— 5%, located on 2 connector pins
—5 Vdc +/— 10%, located on 1 connector pin
+ 12 Vdc +/— 5%, located on 1 connector pin
— 12 Vdc +/— 10%, located on 1 connector pin
GND (Ground), located on 3 connector pins



4-4 Speaker Interface

The sound system has a small, permanent magnet, 2¼ inch speaker. The speaker can be driven from one or two sources:

* An 8255A-5 PPI output bit. The address and bit are defined in the "I/O Address Map"

* A timer clock channel, the output of which is programmable within the functions of the 8253-5 timer when using a 1.19-MHz clock input. The timer gate also is controlled by an 8255A-5 PPI outputport bit. Address and bit assignment are in the "I/O Address Map".

The speaker connection is a 2-pin berg connector, See "System Board Component Diagram", earlier in this section, for speaker connection or placement.